RESEARCH ARTICLE OPEN ACCESS

Modification on Energy Efficient Design of DVB-T2 Constellation De-mapper

Nourhan M Bahgat, Diaa El din S Khalil, Salwa H El-Ramly
Electronics and Communications Engineering Department, Ain Shams University, Cairo, Egypt
Electronics and Communications Engineering Department, Ain Shams University, Cairo, Egypt
Electronics and Communications Engineering Department, Ain Shams University, Cairo, Egypt

Abstract
The second generation of terrestrial digital video broadcasting standard (DVB-T2) offers several advantages for greater efficiency. Signal Space Diversity (SSD) contains rotated constellation and Q-Delay (RQD), which is one of advantage that offered to improve the performance over fading channels compared to the non-rotated modulation. In this journal, the proposed low-power de-mapper design of this work attempts to employ the introduced SSD to reduce power through replacing LLR calculations by a significantly less complex projection-based de-mapping whenever possible. It benefits from an algorithm that applies projection-based de-mapping to significantly reduce LLR computations without deteriorating performance. Two versions are introduced for hard de-mapping and soft de-mapping. The design uses several techniques simultaneously to be even more energy efficient without affecting the performance. Prototype results indicate significant reduction of LLR calculations as Eb/N0 increases with no performance degradation. The idea and energy saving techniques can be easily applied to any rotated constellation de-mapper.

Keywords - DVB-T2, Energy efficient design, FPGA prototype, Rotated constellation, SSD, Statistical LLR assignment.

I. INTRODUCTION

SSD is very effective to improve the system performance in frequency selective terrestrial channels [1-5]. This concept is implemented through the use of rotated constellation and the introduction of Q-delay, where the constellation rotation angle is optimized by the standard to achieve best performance [1].

This journal discusses the implementation of a new DVB-T2 rotated constellation de-mapper which separated to two main parts; the first part benefits from a new algorithm [6] that employs projection-based de-mapping to significantly reduce computational compared to conventional LLR-based de-mapping without deteriorating the performance and the second part benefits from Statistical LLR assignment [7] that employs standard deviation to convert the hybrid output that comes from the first part to soft output to be ready to soft Low Density Parity Check (LDPC) decoder to get the best performance. The proposed DVB-T2 rotated constellation de-mapper output combines between two kinds of outputs. Hard and, soft outputs; hard due to using of scheme-C (all bits comparison) and soft due to normal calculated LLR's thus, all hard bits need to convert to soft through proposed LLR assigning, to be ready for soft LDPC block. Several implementation techniques are also introduced in the proposed design to be more energy efficient as [8]. The proposed implementation benefits from a new algorithm that proposed in [6][7].

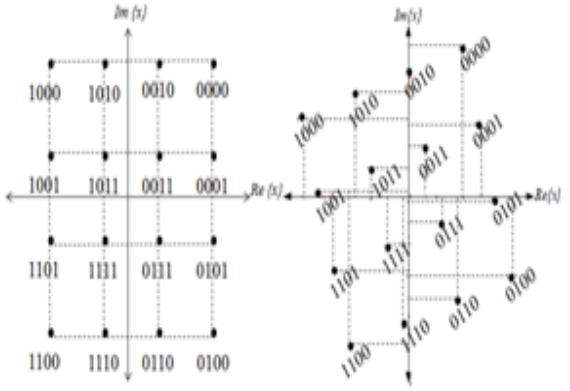
The paper is organized as follows: Section II provides background on the introduced SSD in DVB-T2. Section III explains the Statistical LLR assignment. Section IV explains Standard Deviation Algorithms. Section V highlights prior work in de-mapper implementation. Section VI presents the proposed de-mapper implementation. Section VII, presents the experimental results. And finally, section VIII summarizes the conclusions.

II. BACKGROUND

Applying Bit Interlever Coding Modulation-SSD (BICM-SSD) technique with high modulation diversity and minimum product distance, the performance over a classical Rayleigh fading channel becomes equalize to performance over an Additive White Gaussian Noise (AWGN) channel [1]. The QAM constellation is rotated by an angle ø based on channel type, minimum product distance, and modulation order [1].

Table 1. Optimum angle for different modulation orders [1]

Modulation	QPSK	16-QAM	64-QAM	256-QAM
ø **(degrees)**	29.0	16.8	8.6	$\tan^{-1}(1/16)$



(a) (b)

Figure 1. (a) Classical and (b) rotated constellations

In classical non-rotated 2m QAM, the number of projections to be computed at the de-mapper on both I and Q axes is 2×2m/2. For example, in 16-QAM, m equals 4, then the number of projections are 8, as shown in Fig. 1(a). In rotated 2m QAM, the number of projections to be computed at the de-mapper on both I and Q axes becomes 2m. Due to rotation, each constellation point has a unique projection on each of the I and Q exes. For example, in 16-QAM, m equals 4, then the number of projections are 16, as shown in Fig. 1(b). Such increase in number of projections can be used by the receiver to have more accurate results.

III. LLR BASED DE-MAPPING

The de-mapping proposed in the DVB-T2 standard [1] computes the Log-Likelihood-Ratios (LLRs) for all bits based on the received I and Q components. The exact LLR for a bit bi in the received cell C is given by:

$$LLR(b_i) \approx \ln\left[\frac{\sum_{x\in C_i^1} e^{\frac{(I-\rho_x I_x)^2+(Q-\rho_x Q_x)^2}{2\sigma^2}}}{\sum_{x\in C_i^0} e^{\frac{(I-\rho_x I_x)^2+(Q-\rho_x Q_x)^2}{2\sigma^2}}}\right] \quad (1)$$

Where I and Q are the coordinates of the received cell, Ix and Qx are the coordinates of a certain constellation point x, σ2 is the noise variance, and finally Ci0 and Ci1 are the sets of constellation points having bi equals 0 and 1, respectively. Such complex calculation is usually simplified by the max-log (ML) approximation for a simpler form that is generally more suitable for hardware implementation [9], given by:

$$LLR(b_i) \approx \frac{1}{2\sigma^2}\left[\min_{x\in C_i^0}\left((I-\rho_I I_x)^2+(Q-\rho_Q Q_x)^2\right) - \min_{x\in C_i^1}\left((I-\rho_I I_x)^2+(Q-\rho_Q Q_x)^2\right)\right] \quad (2)$$

It is worth highlighting that even the simplified LLR (2) is still computationally intensive as it involved several multiplication operations for each bit.

IV. PROJECTION BASED DE-MAPPING

LLR based de-mapping technique does not use the uniqueness of the I and Q components (projections) of the rotated constellation points. The main idea of projection based de-mapping is to calculate the closest constellation point (X/Y) to the received cell (I/Q) on each axis separately i.e. the points (X/Y) having minimum 1D distances from the received (I/Q) components to the different (Ix/Qx) projections. The two constellation points corresponding to the minimum distance on each axis are used to make a decision based on a selected scheme. If no decision is possible, the de-mapping falls back to the conventional LLR technique [6]. There are four schemes proposed in [6] for decision. The four schemes are: A (bit-by-bit comparison): Each bit of X is compared with corresponding bit of Y. If they match, such bit value is final. Else, LLR is calculated for that bit. B (bit-by-bit comparison excluding weak points): If either X or Y belongs to weak points, then all bits are calculated by conventional LLR. Else, scheme A is applied. A weak point on an axis is a point having its projection rather close to its neighbor compared to other points on that axis. C (all-bits comparison): All bits of X are compared with corresponding bits of Y. If they match, all bit values are final. Else, LLR is calculated for all bits. D (single-axis for weak points): If X (or Y) belongs to weak points, and then all bits of Y (or X) are final. Else, scheme A is applied. Such four schemes actually present different points of trade-off between reducing computational complexity and maintaining BER performance. Scheme C (all-bits comparison) is adopted for the proposed de-mapper implementation since it demonstrated the best BER performance that matches the reference performance of all-bits LLR de-mapping [6]. Fig. 3 presents an illustrative flowchart for the adopted scheme C.

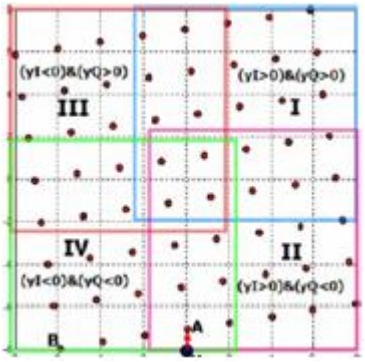


Figure 2. Sub-regions of rotated QAM-64 constellation [8]

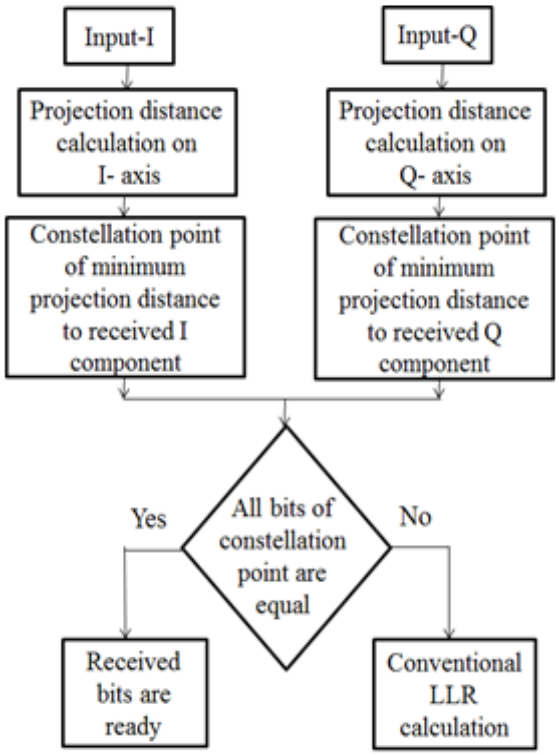


Figure 3. Flowchart for scheme C of [6] (all-bits comparison)

V. STATISTICAL LLR ASSIGNMENT

High performance communication system use soft decoding in the receiver. In such case, hard bits from projection based de-mapping need to be converted to LLRs before passing to subsequent blocks as illustrated in Fig 4 for DVB-T2 system. A simple assignment of maximum and minimum LLR values to 1 and 0 respectively does not give optimum BER performance and an elaborate statistical calculation is required to achieve best BER performance [7]. Since, the proposed de-mapper benefits from projection based de-mapping to save calculations and energy, the output of such de-mapper will be hybrid combination between hard bits and soft LLR values. If the de-mapper is followed by hard LDPC decoder a simple comparator can be used to make the hard decision for LLR values. However, if the de-mapper is followed by soft LDPC decoder, the statistical calculations must extract the LLR values of the output to perform the calculation and also extract the hard bits to replace [7] Fig 5 illustrates the process.

The hybrid output of the de-mapper contains; the soft outputs (LLR's) represented by the symbols (S1, S2, S4) and the hard outputs (bits) represented by the symbols (H3, H5). The separator is used to split the input stream into two sub-streams. The soft outputs sub-stream has only the S symbols and the hard outputs sub-stream has only the H symbols. The output soft data pass to statistics calculation block to calculate mean and standard deviation per FEC frame [7]. These values are used to perform LLR assignment of the separated hard bits in the next FEC frame. The merger block combines between the assigned values representing the hard bits into their position to form a stream of all soft outputs.

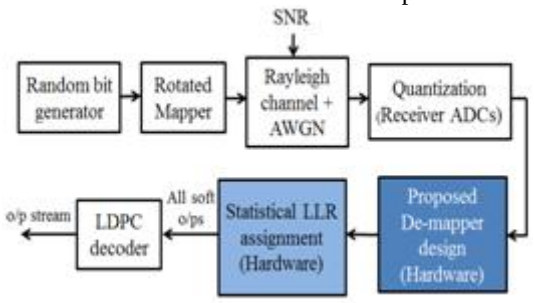


Figure 4. Statistical LLR assignment

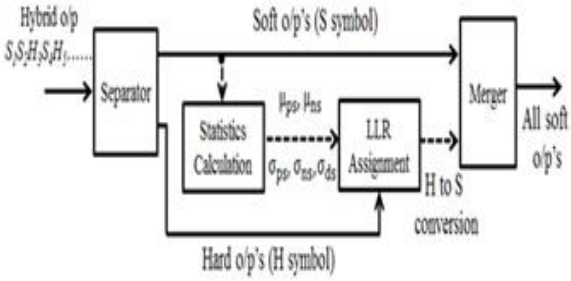


Figure 5. Statistical LLR assignment block diagram [7]

In [7], two techniques are proposed for standard deviation calculations. One is the double sided standard deviation (σ_{ds}), where standard deviation is calculated for all LLR values. The other is the single sided standard deviation, where two standard deviation are calculated for the positive and negative LLRs (σ_{ps},σ_{ns}). No difference in performance exists between the two techniques [7]. In our proposed implementation the single sided technique is adopted to allow combined calculations to save energy.

The LLR assigned values (LLR_{est}^{1}, LLR_{est}^{0}) calculated for the 1's and 0's independently. Each one depends on its corresponding mean and standard deviation as given in the following equations [7]:

$$LLR_{est}^{1} = \mu_{ps} + c.\sigma_{ps} \quad (3)$$

$$LLR_{est}^{0} = \mu_{ns} + c.\sigma_{ns} \quad (4)$$

$$C = \begin{cases} 2.883, & SNR \leq 5 \\ 5.11 - 0.474\,SNR, & SNR > 5 \end{cases} \quad (5)$$

where σ_{ps} is the positive LLRs distribution standard deviation, σ_{ns} is the negative LLRs distribution standard deviation, μ_{ps} is the mean of the positive side (the ones) of the LLR histogram distribution. μ_{ns} is the mean of the negative side (the zeros) of the LLR histogram distribution and c is the Empirical scaling factor. The empirical equation obtained by analyzing performance for different SNR values. The optimum c equation is divided into two parts depending on the SNR range. For SNR values from 0 to 5 dB, the optimum c is constant while for SNR > 5dB, the optimum c is dependent on SNR as given in (3) [7].

VI. PRIOR WORK IN IMPLEMENTATION

The most relevant work has been recently published by [8]. It proposes a new de-mapper design that reduces the computational effort of LLR calculations by reducing the set of distance calculations based on the signs of the received I and Q. For 64-QAM and 256-QAM, the constellation space is divided into four sub-regions as shown in Fig. 4. Based on the signs of the received I and Q, one sub-region is selected for LLR calculations rather than the whole constellation space. Hence, the number of distances in LLR calculations is reduced. In addition, it proposes a simple approximate formula for Euclidean distance calculation that gets rid of multiplication operations and further reduces the computational effort of LLR calculations, given by:

$$D(a,b) \approx \begin{cases} \max(a,b) \; ; \min(a,b) \leq \frac{\max(a,b)}{4} \\ \max(a,b) + \frac{\left(\min(a,b) - \max\frac{(a,b)}{4}\right)}{2} \; ; otherwise \end{cases} \quad (6)$$

VII. PROPOSED IMPLEMENTATION

In this work, a new energy efficient design of the DVB-T2 constellation de-mapper is presented and prototyped. It leverages the benefit of significantly lower computational effort of projection-based de-mapping to avoid the rather large computation effort of LLR calculation whenever possible, allowing all LLR calculation blocks to be clock-gated. Also, it reduces the computational effort of LLR calculation by using the simplified Euclidean distance of [8] and by a proposed efficient minimum search technique that combines distance calculation with minimum search to get rid of all intermediate distance storage and by a pipelined use of multipliers. The design supports all modulation types in DVB-T2 standard, namely QPSK, 16-QAM, 64-QAM, and 256-QAM through a 2-bit selector. Also, it is reconfigurable where projection-based de-mapping can be activated or not through an enable. In case projection-based de-mapping is deactivated, the related blocks are clock-gated. Received I and Q are 9 bits each for high enough resolution. Each LLR value is 11 bits to accommodate all values without truncation.

Fig. 6 presents a block diagram that illustrates the proposed de-mapper design. The de-mapper gets I and Q bits from the cell de-interleaver. The (control block) passes them to the two (minimum projection distance calculators) and clock-gate all LLR related blocks. Once the X-bits and Y-bits, corresponding to the nearest constellation point projections on the I and Q axes respectively, are calculated, a (comparator) is used to check for matching. If they match, the bits are final and no need for LLR calculations, so the LLR related blocks remain clock-gated. If they are different, a flag is asserted to (control block) to enable the LLR related block and pass the stored I and Q bits to them. The two (minimum Euclidean distance calculators) compute the minimum distances for the Ci0 and Ci1 sets of constellation points using the simplified formula of (3). Then the (LLR calculator) computes the LLR values for each bit according to (2). And finally, a (hard decision) circuit converts LLR values to bits. After the LLR calculations are done the (control block) clock-gates the related blocks again. A pipelined minimum search technique is implemented in all the four minimum distance blocks. It combines the distance calculation steps with on-the-fly minimum search algorithm that updates the minimum value once a new distance is ready. Such design eliminates the need for distance storage, hence reduces hardware significantly. Also, it achieves the best latency reaching the minimum distances as it just takes one extra clock cycle after last distance calculation.

Fig 7 presents a block diagram that illustrates the proposed statistical LLR assignment design. The design separates the hybrid input stream to three sub-streams one for soft (LLRs), other sub-streams for hard bits, one of them for zero hard bit and another for one hard bits. The soft (LLRs) passes to LLR separator block to separate it to two passes, one for LLR which represent one (LLR > 0) and another for LLR which represent zero (LLR ≤ 0) to calculate mean and standard deviation for positive and negative sides to calculate LLR_{est}^{1} and LLR_{est}^{0} with (1), (2). Empirical scaling factor block, out its value depends on SNR value. Finally, the mux block combines LLRs from three paths (original soft, LLR_{est}^{1} and LLR_{est}^{0}) and merges them correctly in order to be ready to soft LDPC block.

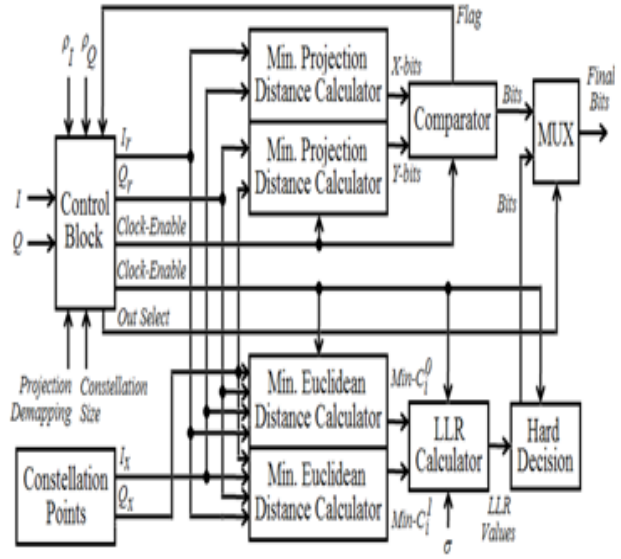


Figure 6. Block diagram of the proposed de-mapper design

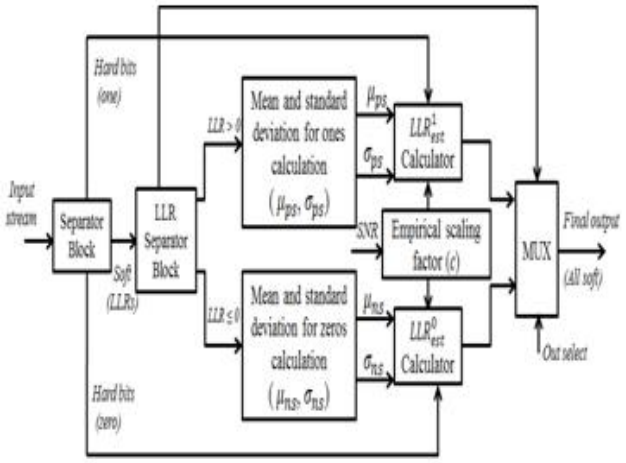


Figure 7. Block diagram of the proposed statistical LLR assignment

The Empirical factor (c) shown in (5) is complex to implement because it contains real numbers. To avoid any use of real numbers and multiplications/divisions, (5) is converted to (7) through approximations and introducing a factor of 16. This factor preserves the accuracy of having decimal fractions of original equation and is reversed after multiplication by the standard deviation in LLR calculations simply using shift operation.

$$C = \begin{cases} 46, & \text{SNR} \le 5 \\ 84 - 8\,\text{SNR}, & \text{SNR} > 5 \end{cases} \quad (7)$$

While [7] calculates the mean and standard deviation for each FEC frame (16200 bits), this work proposes to do the calculations on small sub-frames each is 1024 bits that is a power of 2 for binary numbers. The mean divided by shift operation. The sub-frame is more accurate than FEC frame (16200 bits) because the mean on few values give more accuracy. The basic operations like addition and subtraction are easy to implement in an FPGA because synthesis tools have optimized addition/subtraction units based on FPGA architecture. Multiplication, division and square root are complex operations; square root in particular, is computationally intensive as it involves convergence and approximation techniques. Many algorithms have been developed to implement it on FPGAs. But there is a need of an algorithm which should be more efficient in terms of time, speed and area. Thus, to calculate the square root of standard deviation in this energy efficient design an approximation is needed to reduce it to simple formulas that only uses addition, subtraction, and shift. After plotting the square root function, it could be simplified as follows: The function is split into three ranges as represented in equation (8). The first range from 0 to 2048, is difficult to approximate. However to avoid complex calculations, it is saved as 12-bit LUTs. The second range from 2048 to 8192 and the third range from 8192 to 16383 use linear approximation and hence reduce hardware and guarantee the speed.

$$\sigma = \begin{cases} LUTs, & 0 \le range < 2048 \\ (\sigma^2/128) + 30, & 2048 \le range < 8192 \\ (\sigma^2/256) + 62, & 8192 \le range \le 16383 \end{cases} \quad (8)$$

The proposed de-mapper is implemented as VHDL then synthesized and prototyped on VertixII-pro FPGA XC2VP30 (same as [8] for comparison). Table 2 presents the FPGA hardware resources utilization in the proposed design as well as the reference design [8] for comparison. Hardware overhead of projection based de-mapping is only 12% compared to LLR blocks. Hence, energy overhead is roughly estimated as 12% when projection-based de-mapping is inconclusive and LLR de-mapping has to be used. On the other hand, energy saving is roughly estimated as 88% when projection-based de-mapping is conclusive and LLR de-mapping is not used. The actual energy saving is actually less considering the leakage power dissipated whether clock-gating is applied or not.

Compared to [8], the hard de-mapper proposed design, with the projection-based de-mapping overhead and with Euclidean distance calculation for all constellation points, uses 40% less hardware. This is mainly attributed to the efficient minimum search technique and the pipelined use of multipliers. Such hardware reduction directly translates to energy saving since the same clock speed is used in both designs and both meet the latency constraint imposed by cell duration from standard.

In this work also, a design of statistical LLR assignment is proposed to utilize the concept of single-sided standard deviation algorithm not double-sided standard deviation algorithm to combine calculation of standard deviation (σ). The proposed Statistical LLR assignment is implemented as VHDL then synthesized and prototyped on VertixII-pro FPGA XC2VP30. Table 3 presents the FPGA hardware resources utilization in the proposed design.

Table 2. The FPGA hardware resources without statistical LLR assignment

Hardware Resources	Hard De-mapper Proposed Design		Design of [8]
	Scheme-C and LLR blocks	LLR blocks	
LUTs	2,928	2,559	4,667
Flip-Flops	1,741	1,328	791
DSP blocks (multipliers)	8	8	20
Memory blocks	0	0	0

Table 3 The FPGA hardware resources with statistical LLR assignment

Hardware Resources	Soft De-mapper Proposed Design		Design of [8]
	Full	Statistical LLR assignment block	
LUTs	3,280	658	4,667
Flip-Flops	1,814	281	791
DSP blocks (multipliers)	13	5	20
Memory blocks	0	0	0

It is worth highlighting that no memory blocks are used in soft de-mapper proposed design since all standard deviation probabilities values are stored in registers to improve speed and simplify design and further from the root as possible. Adding the proposed Statistical LLR assignment to propose design of DVB-T2 rotated constellation hard de-mapper is implemented as VHDL then tested by Modelsim simulation then synthesized and prototyped on VertixII-pro FPGA XC2VP30. Table 3 presents the FPGA hardware resources utilization in the proposed design. It is worth highlighting that proposed full design (soft de-mapper) or (the proposed statistical LLR assignment with proposed DVB-T2 rotated constellation de-mapper) still less than [8]. Thus, it is still more efficient energy. The full system (the proposed Statistical LLR assignment with proposed design of DVB-T2 rotated constellation de-mapper) saves 22% more than [8] in hardware resources. The proposed Statistical LLR assignment with proposed design of DVB-T2 rotated constellation de-mapper (soft de-mapper) saves almost 36 % when projection-based de-mapping is conclusive and LLR de-mapping is not used.

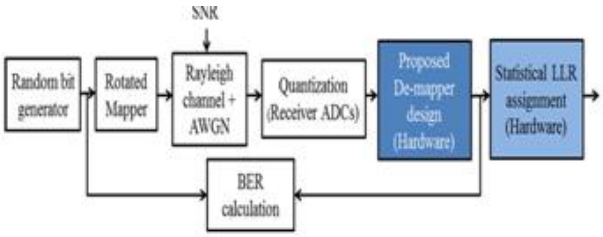


Figure 8. The experimental measurement setup

VIII. EXPERIMENTAL RESULTS

An experimental measurement setup is used to simulate the hardware performance of the proposed design. While the DVB-T2 system obviously has complex bit-chain processing steps, the steps performed at transmitter are sequentially reversed at the receiver. Hence, it is acceptable to only consider the processing steps related to the block under inspection. As a result, in the measurement setup, a mapper is used with random bits, followed by channel model and additive white Gaussian noise (AWGN), then quantization representing the receiver ADCs, before entering the de-mapper. Fig. 8 illustrates the experimental measurement setup. Matlab is used to generate I and Q bits going into the de-mapper hardware and perform BER calculations. A random data bits stream is generated then passed through an ideal mapper to generate I and Q values of corresponding cells to be transmitted. The cells pass through a classical Rayleigh channel with no erasure. Then, AWGN is added with controlled SNR level. The resultant I and Q values are then quantized into 9 bits each (same as hardware design). The data are then passed to Modelsim to simulate the de-mapper hardware. Finally, the de-mapped bits are passed back to Matlab for BER calculation.

Experimental results for 64-QAM are presented in this section for illustration. Fig. 9 plots the BER vs. Eb/N0(dB) for the proposed prototype simulation with projection-based de-mapping activated and disabled, along with ideal Matlab simulation of LLR based de-mapping. In addition, it presents the prototype simulation and the ideal Matlab simulation of [8] for comparison.

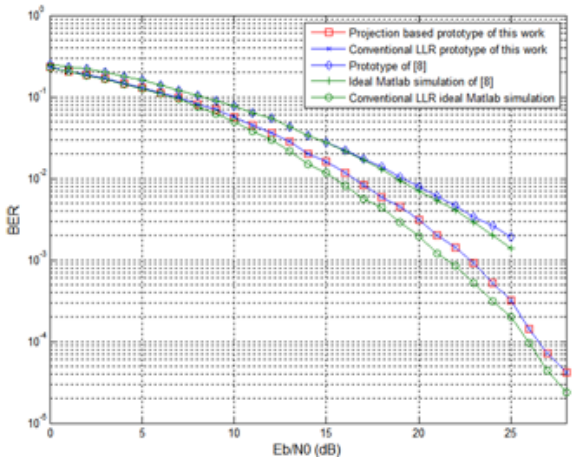


Figure 9. BER performance comparison for 64-QAM

It is worth highlighting that the simulations of [8] are not repeated. The curves data are exactly copied from the relevant figure in [8]. No impact on BER performance is observed when using projection based de-mapping vs. LLR based de-mapping for all cells. This agrees with reference [6]. This can be attributed to the conservative projection-based de-mapping scheme used. Projection-based de-mapping is only used when noise is rather low that both received I and Q projections are closest to correct constellation point. So, the probability of incorrect decision is very low. Both curves of the proposed prototype simulation are close to LLR ideal Matlab simulation with observed increase in BER resulting from quantization, which is not represented in such ideal Matlab simulation. BER performance of the proposed prototype is better compared to that of [8]. This can be attributed to the reduced subset of constellation points used in [8] to reduce LLR calculations as explained in section VI.

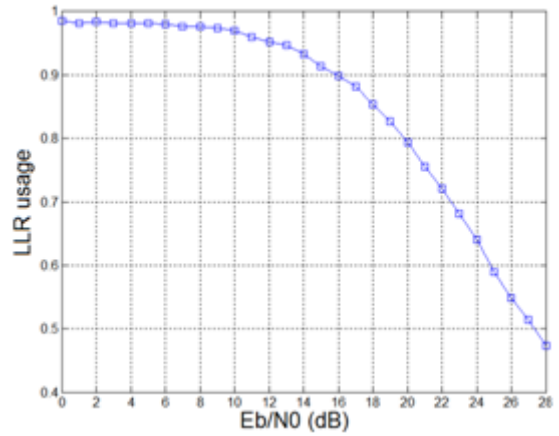


Figure 10. LLR usage vs. Eb/N0 values

The proposed Statistical LLR assignment is implemented as VHDL then tested by Modelsim simulator. Fig. 11 illustrates simulation results of the statistical LLR assignment, while the design is verified to work correctly in simulation. In simulation the reset is used for initial state, when (reset=”1”), the system reset; but when (reset=”0”), the system waits the rising edge of clk to work. The snr (signal-to-noise ratio); is the system input which is function in empirical factor (c). llr signal is the system input (soft input which it comes from separator block), Count_one and count_zero signals count positive and negative input LLRs. The sum_llrs_one, sum_llrs_ zero, sum_squred_llr_one, sum_ squred_ llr_ zero signals are intermediate signals that used to calculate mean and standard deviation for the 0 and 1 independently. The est_llr_one and est_llr_zero signals; are the system output. Thus, the design implement LLR_{est}^{1} and LLR_{est}^{0} which shown in (3), (4). It is also important to evaluate the computational effort reduction and corresponding energy saving, as well as, to highlight their dependence on Eb/N0. With the conservative projection-based de-mapping scheme used, LLR calculations are skipped only when noise affecting the cell is low enough that both projections lead to same constellation point. The probability of such case certainly increases as Eb/N0 increases.

Fig. 10 presents the normalized LLR usage vs. Eb/N0(dB). When Eb/N0 is small, the received data is rather noisy and projection based de-mapping will only succeed in very few cells while LLR calculations will be needed for almost all cells. As Eb/N0 increases, the data becomes less noisy and projection based de-mapping will succeed with more cells, saving more LLR calculations. Such saving continues to improve significantly as Eb/N0 continues to increase as indicated in Fig. 8 thus it normalized the usage of LLR; hence benefits from projection based de-mapping and clock-gate all LLR calculation blocks. For example, at Eb/N0 of 27dB, the proposed design saves almost half of the LLR calculations. This translates to roughly 44% of energy saving. (As estimated in section VII, 88% energy saving is achieved when LLR calculation is skipped).

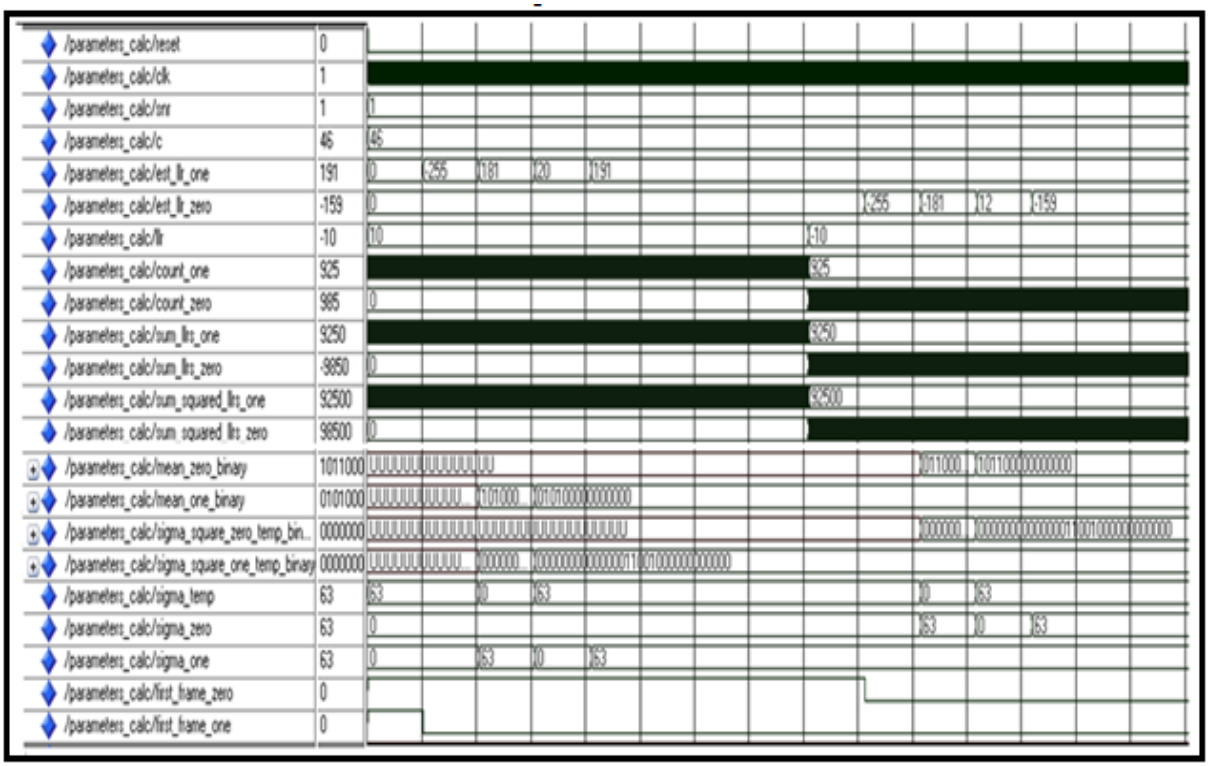


Figure 11. The proposed Statistical LLR assignment

IX. HARDWARE IMPLEMENTATION

FPGA's are equipped with a lot of resources that allow them to hold large digital systems on a single chip. FPGA vendors provide tools that allow the designer to build embedded systems on FPGAs. One of the new concepts that discuss in this experiment is the System-on-Chip approach (SoC). Xilinx provides a tool for building an embedded SoC on its FPGAs, and we are going to use this tool in this experiment. This tool is called Xilinx Embedded Development Kit (EDK). The EDK allows the designer to build the processor system based on an embedded processor in Xilinx called MicroBlaze. The tool provides a C/C++ compiler for the processor and VHDL/Verilog for coprocessor.

In this journal, we changed C program to adopt proposed de-mapper. Make the serial port transmit two input numbers and receive one output then test it, I/O display on "Hyper Terminal" or "Matlab". While the C program is verified to work correctly in simulation, start to change VHDL code to proposed de-mapper. The VHDL code in MicroBlaze writes as finite state machine. The problem in the VHDL code template is that the result is immediately written after the last input is read. However, proposed de-mapper depends on clock cycle. To overcome this problem, add a new state to the state machine, and modify the state transitions to introduce this new state between the "Read_Inputs" and "Write_Outputs" states. The new state in this project called "processing" state that depends on FSL (Fast Simplex Link) bus clock (FSL_CLK). The FSL bus provides a point to point communication between any two peripherals modules on the FPGA. To write output, the flag up to transit to "Write_Outputs" state as illustrate in Fig.12.

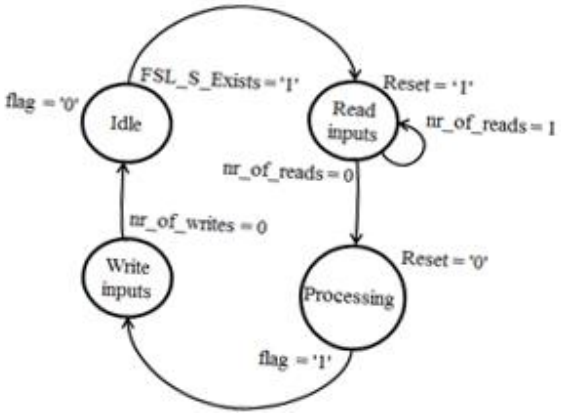


Figure 12 Proposed de-mapper finite state machine

In the beginning, Generating bit stream for proposed de-mapper hardware implementation. The hardware synthesized on Xilinx VertixII-pro FPGA XC2VP30. Table 4 presents the FPGA hardware resources utilization in the hardware proposed design.

Table 4 The FPGA hardware resources for EDK tool

Hardware Resources	64-QAM with serial port
LUTs	2,303
Flip-Flops	1,849
DSP blocks (multipliers)	3
Memory blocks	4

X. CONCLUSION

Two versions are introduced for DVB-T2 rotated constellation de-mapper, hard de-mapping and soft de-mapping. Proposed design of hard de-mapper is presented and prototyped. The design benefits from projection based de-mapping to significantly reduce power by saving LLR calculations. It also used several techniques to be even more energy efficient. Experimental results clearly indicate there is no performance degradation when projection based de-mapping is used. Experimental results also indicate significant reduction of LLR calculations and corresponding energy saving as Eb/N0 increases. Proposed design of soft de-mapper is presented and prototyped. [7] presents two algorithms to transform from the hybrid output stream from proposed hard de-mapper to all-soft stream in order to guarantee the best performance of the soft LDPC decoder. These two algorithms were tested and gave almost the same performance at low SNR values and a slightly better performance at a moderate SNR range so, the proposed design of statistical LLR assignment utilize the concept of single-sided standard deviation, prototyped by VHDL and simulated by Modelsim. The proposed full system (soft de-mapper) saves almost 36 % from energy when LLR calculation is skipped.

REFERENCES

[1] Digital Video Broadcasting (DVB); Frame structure channel coding and modulation for a second generation digital terrestrial television broadcasting system (DVBT2), ETSI Standard EN 302-755, v1.2.1, Feb. 2011.

[2] J. Boutros, E. Viterbo, "*Signal space diversity: A power and bandwidth-efficient diversity technique for the Rayleigh fading channel*," Transactions on Information Theory, vol. 44, no. 4, pp. 1453-1467, Jul. 1998.

[3] X. Giraud, E. Boutillon, and J. C. Belfiore, "*Algebraic tools to build modulation schemes for fading channels*," Transactions on Communications, vol. 43, no. 3, pp.938–952, May 1997.

[4] C. Abdel Nour and C. Douillard, "*Rotated QAM Constellations to Improve BICM Performance for DVBT2*," International Symposium on Spread Spectrum Techniques and Application, pp. 354-359, Aug. 2008.

[5] C. Abdel Nour and C. Douillard, "*Improving BICM performance of QAM constellations for broadcasting applications*," International Symposium on Turbo Codes and Related Topics, pp. 55-60, Sep. 2008.

[6] M.Z. Saleh, M. Sadek, S.H. Elramly, "*Novel hybrid soft hard demodulation schemes for RQD constellation*," International Conference on Telecommunications and Signal Processing, pp. 684-688, Jul. 2012.

[7] M.Z. Saleh, M. Sadek, S.H. Elramly,"*A Modified Hybrid RQD Demapper based on Novel Hard to Soft Assigning Algorithm*, "In Application of Information and Communication Technologies (AICT), 7th International Conference on (pp. 1-6). IEEE, October 2013.

[8] M. Li, C. Abdel Nour, C. Jego, C. Douillard, "*Design of rotated QAM mapper/demapper for the DVB-T2 standard*," Workshop on Signal Processing Systems, pp. 18-23, Oct. 2009.

[9] Digital Video Broadcasting (DVB); Implementation guidelines for a second generation digital terrestrial television broadcasting system (DVB-T2), DVB Document A133, Feb. 2012.

[10] M. Li, C. Abdel Nour, C. Jego, J. Yang, C. Douillard, "*Design and FPGA Prototyping of a bit-interleaved Coded Modulation Receiver for the DVB-T2 Standard*", Workshop on Signal Processing Systems, Nov. 2010.

[11] M. Li, C. Abdel Nour, C. Jego, J. Yang, C. Douillard, "*FPGA implementation of a shuffled iterative Bit-Interleaved Coded Modulation receiver*," Workshop on Signal Processing Systems, Oct. 2011.